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Design And Implementation Of Low Power Multiplier Using Reversible Logic Gates

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Abstract: *Reversible logic is one of the important technologies for low power dissipation. Reversible logic gates aims at optimizing the delay, area and power consumption. The normal set of gates such as the NAND, AND, NOR, OR, XOR and XNOR are not reversible because number of inputs and outputs are not equal, in reversible logic gates number of inputs is equal to number of outputs. Some of the reversible logic gates are Feynman gate, Fredkin gate, Double Feynman gate, Toffoli-Gate, Peres gate and HNG gate. Power consumption is one of the major drawbacks in the multiplier. Power consumed by the multiplier is higher in the digital circuits. To overcome the power consumption problem by design an efficient low power multiplier. The low power multiplier is designed by using reversible logic gates. Generally reversible logic was designed to avoiding the higher power consumption in the circuits, compared to Irreversible logic gates, reversible logic consumes less power. To apply the logic in the entire multiplier circuit and see the performance of the multiplier. The low power multipliers overcome the power dissipation in the circuits. The designs are done by low power CMOS circuit and Implemented by Tanner EDA simulation environment. The power can be analyzed by using T-spice analysis. Finally comparison is done between the irreversible and reversible design.*

Keywords: *Low power multiplier, Reversible Logic gates, Tanner EDA, CMOS, T-spice.*

I. Introduction

In VLSI system the power-delay product become the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimization at all levels of the design procedure. Since, most digital circuitry is composed of simple and/or complex gates.we study the best way to implement multiplier in older to achieve low power dissipation and high speed.

In 1960 R. Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kT1n2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed. In 1961, a physicist from IBM called Rolf Landauer proved that when data is lost in an irreversible circuit, that data is dissipated in the form of the heat. For this reason the scientific community has shown continuous interest in matching the already existing logic principles to avoid the No-Free-Lunch theorem as much as possible.Reversible logic theoretically allows designers to build subsystem circuits design with zero power dissipation than the existing classical ones. Reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. Reversible gates require constant inputs for reconfiguration of gate functions and garbage outputs that help in keeping reversibility. It is important to minimize parameters such as constant and garbage bits, quantum cost and delay in the design of reversible circuits.

II. Reversible Logic

An n-input n-output function F is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs. Therefore, the input vector can be uniquely determined from the output vector.

2.1reversible Logic Gates

Reversible logic may be a promising computing style paradigm that presents a way for constructing computers that manufacture no chilling. Reversible computing emerged as a result of the applying of quantum physics principles towards the event of a universal computer. Specifically, the basics of reversible computing are supported the link between entropy, heat transfer between molecules during a system, the chance of a quantum particle occupying a specific state at any given time, and also the quantum field theory between electrons once they are in dose proximity. the essential principle of reversible computing is that a objective device with an even range of input and output lines can manufacture a computing surroundings wherever the electrodynamics of the system allow prediction of all future states supported illustrious past states, and also the

system reaches each attainable state, leading to no chilling .Generally reversible logic gates characteristics are defined as follows-

- Total number of input signals = total number of output signals.
- One to one mapping between input and output variables.
- No feedback.
- Individual output bits are high for a total of n/2 times for atotal of n input combinations.
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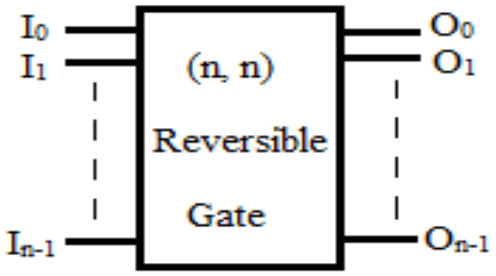

Fig.1: Block diagram of (n, n) reversible logic gate

In reversible logic we have one more factor, which is more important than the number of gates used, namely the number of garbage outputs.The unutilized outputs from a reversible gate/circuit are called "garbage". Though every synthesis method engages them producing less number of garbage outputs, but sometimes garbage outputs are unavoidable. A reversible computer circuit is associate degree N-input N-output logic device that has one to 1 mapping between the input and also the output. Garbage outputs are those that don't contribute to the reversible logic realization of the look. Quantum solid refers to the value of the circuit in terms of the value of a primitive gate. Gate count is that the range of reversible gates wont to understand the operate. Gate level refers to the amount of levels that are needed to understand the given logic functions. The following are the necessary style constraints for reversible logic circuits.This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates.

- Reversible logic gates don't permit fan-outs.
- Reversible logic circuits ought to have minimum quantum price.
- The look is optimized thus on manufacture minimum range of garbage outputs.
- The reversible logic circuits should use minimum range of constant inputs.
- The reversible logic circuits should use a minimum logic depth gate levels.

2.2 Reversible Logic Implementation Of Full Adder Circuit

Full adder is the fundamental building block in many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible reversible adder implementations. The full adder circuit's output is given by the following equations:

Sum=A xor B xorCin …. (1)

Cout= (A xor B) CinxorAB …. (2)

Any reversible logic realization of full adder circuit includes at least two garbage outputs and one constant input. It has given a quantum cost efficient reversible full adder circuit that is realized using two 3*3 Peres gates only This implementation of reversible full adder circuit is also efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.

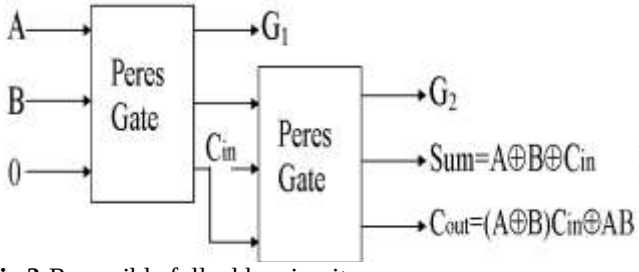

Fig.2: Reversible full adder circuit

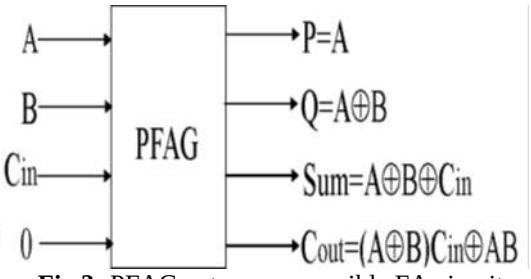

Fig.3: PFAG gate as a reversible FA circuit

Full adder is the fundamental building block in almost every arithmetic logic circuit. Therefore, a gate that can work singly as a reversible full adder will be beneficial to the development of other complex logic circuits. This paper presents a novel reversible full adder gate namely Peres Full Adder Gate (PFAG). The gate is achieved by cascading two 3*3 Peres gate.

III. Multipliers

Multiplier is an important hardware unit that decides the speed in any processor .Multiplication is the most important arithmetic operation in signal processing applications. All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement.

Let us consider two inputs *X*1*X*0 and *Y*1*Y*0, each of 2 bits. *P*3*P*2*P*1*P*0 represents each bit of the final computed product.The result is obtained after generating partial products and adding them as per the basic method of multiplication shown below.

*X*1 *X*0
× *Y*1 *Y*0
−−−−−−−−−−−−−−−−
*X*1*Y*0*X*0*Y*0
*X*1*Y*1*X*0*Y*1
−−−−−−−−−−−−−−−−
P3 *P*2 *P*1*P*0

3.1vedic Multiplier

Multipliers are most often used in digital signal processing applications and microprocessors designs. In contrast to process of addition and subtraction, multipliers consume more time and more hardware resources. With the recent advances in technology, a number of multiplication techniques have been implemented for fulfilling the requirement of producing high speed, low power consumption, less area or a combination of them in one multiplier. Speed and area are the two major constraints which conflict each other. Therefore, it is the designer's task to decide proper balance in selecting an appropriate multiplication technique as per requirements.

Parallel multipliers are the high speed multipliers. Therefore, the enhanced speed of the multiplication operation is achieved using various schemes and Vedic is one of them. There are three phases in the multiplier architecture:

1. The first phase is the generation of partial products.
2. Accumulation of partial product in second phase.
3. The third phase is the final addition phase.

Fig.4 shows the Vedic construction method is usually preferred to add the partial products in a tree-like fashion. The method used to construct the Vedic considers all the bits in each four rows at a time and compress them in an appropriate manner.

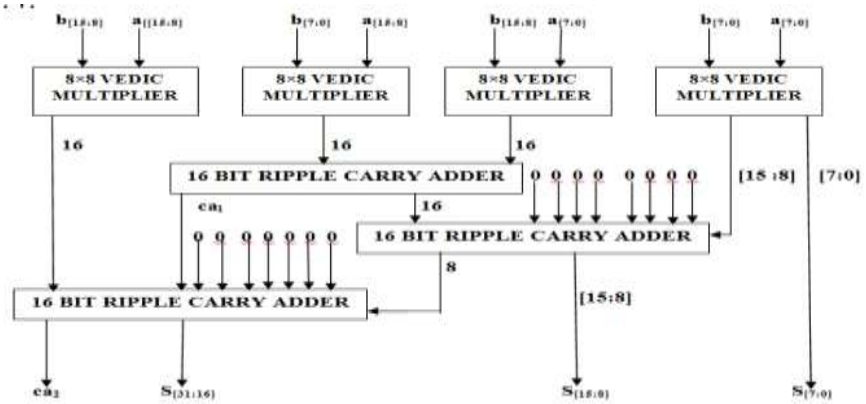

Fig.4: Block Diagram of Vedic Multiplier

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and

performance it include the area like Low power CMOS,Design of low power arithmetic and data path for digital signal processing (DSP),Field Programmable Gate Arrays (FPGAs) Other DSP applications such as Convolution.,Fast Fourier Transform (FFT).,Discrete Cosine Transform (DCT) and Filtering.

3.2 16-Bit Multiplier Using Reversible Logic Gates

In the 16 bit vedic multiplier, there are four 8x8 multipliers are used for multiplying the given two 16 bit inputs (i.e) A and B. For each 8x8 multiplier two 8bits are given as input from A and B.The partial products are added using ripple carry adder.Since the inputs are 16 bits ,16 bit ripple carry adder is used to add the partial product generation.One of the 8x8 vedic multiplier gives the direct output of p[7:0].the outputs of two 16-bit Ripple Carry Adder is given as an input to an another 16-bit Ripple Carry adder which gives outputs p[32:8].

The Block diagram of the Existing and the Proposed system are almost similar and the efficiency of reversible logic gates are large when compared to the irreversible multiplier mainly because of the use of the Peres full adder Gate (PFAG Gate).Zero Padding can also be done in order to give 16-bit inputs to the Ripple Carry Adder.

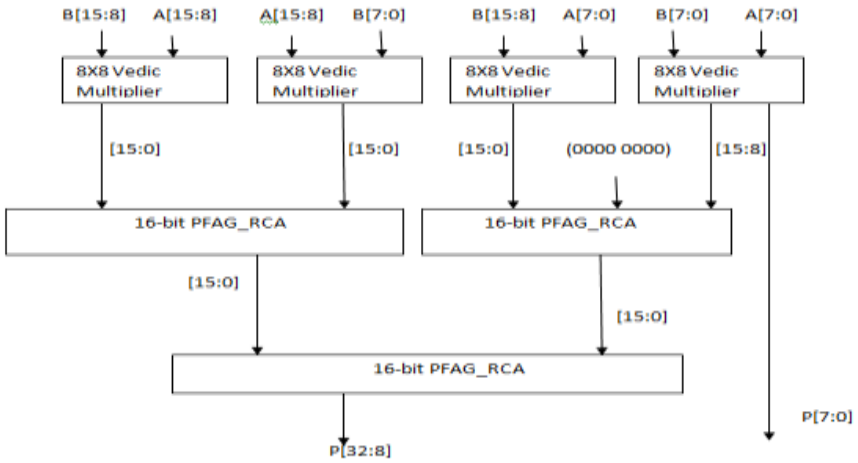

Fig.5:16-Bit Multiplier Using Reversible Logic Gates

IV. Results And Discussion

4.1simulation Of 16-Bit Irreversible And Reversible Vedic Multiplier

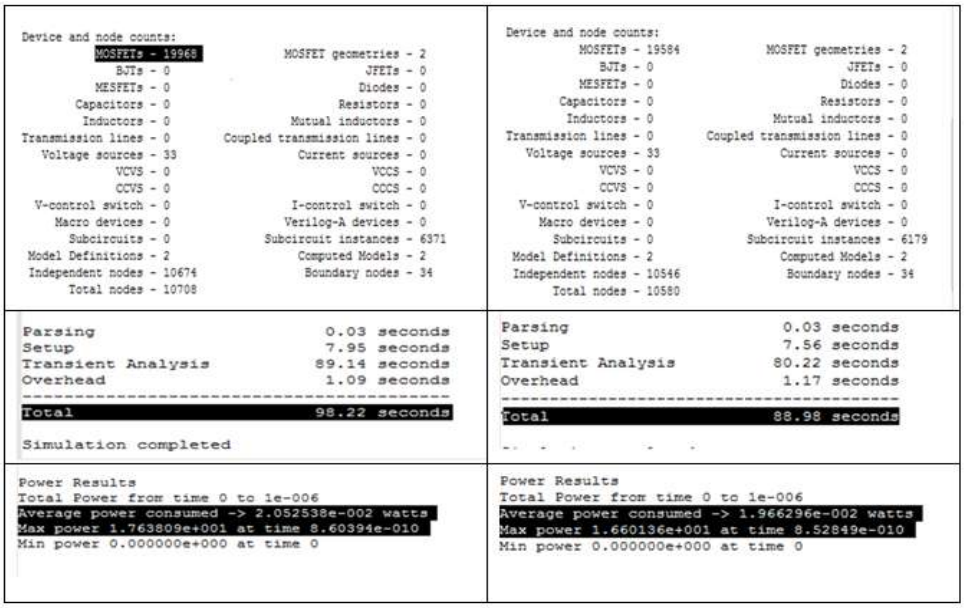

Fig.6: Area, delay and power analysis of 16 bit Vedic multiplier

4.2 Comparison Between 16 Bit Irreversible And Reversible Multiplier

Parameters	Vedic multiplier using Reversible logic	Existing Vedic multiplier
Total number of MOSFETs used	19584	19968
Time(seconds)	88.98s	98.22s
Power(watts)	1.96629e-002w	2.052538e-002w

Table.1: Comparison between Irreversible and Reversible Multipliers

The above table clearly shows that the comparison between the multipliers. From this comparison the number of transistor counts decreased and the ADP products can be analysed. From the above multipliers, the reversible Vedic multiplier gives less transistor count 19584 as compared to the existing Vedic multiplier count as 19968.The time and power product for the proposed system are 88.98 s,1.96629e-0.02w.

V. Conclusion

The low power multiplier is designed to get an efficient FIR using a reversible logic gates. Among Various reversible logic gates in this project Peres full adder gate is used to reduce the power consumption .The Peres reversible full adder gate act as a reversible full adder circuit.

The proposed reversible Vedic multiplier uses less number of transistors as compared to Vedic multiplier. Irreversible Vedic multiplier uses 19968 transistors and reversible Vedic multiplier uses 19584 transistors as comparing with the existing system the proposed system reduces 384 transistors. As compared with the existing system the proposed system reduces 4.2% of power. It reduces the power consumption as compared to the Wallace multiplier. Hence the reversible multiplier uses low power consumption.

The reversible multiplier is designed and analyzed. As compared to irreversible Vedic multiplier, the reversible Vedic multiplier provides efficient result. The area, delay and power product are analyzed using T-spice.

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